In the claims:

Please amend the claims as follows:

1. (Currently Amended) A semiconductor device comprising:

a plurality of regions representing output bits; and

a dummy pattern having the same shape as the output bits formed to be adjacent to the end portion of a output bit group.

2. (Original) A semiconductor device for a driver comprising:

a plurality of output one bits constituting an output bit group; and

a dummy pattern having the same shape as the output bits formed to be adjacent to the end portion of the output bit group.

3. (Original) The semiconductor device according to claim 2, wherein the dummy pattern is formed at an empty space in a region where a plurality of output bits are arranged.

4. (Original) The semiconductor device according to claim 2, wherein the dummy pattern is formed to be adjacent to the end portion of each output bit group constituting a cathode driver, an anode driver and an anode driver for icon.

5. (Original) The semiconductor device according to claim 4, wherein number of outputs of the dummy pattern formed at a region where output bit groups constituting the cathode driver, the anode driver and the anode driver for icon are adjacent each other is less than number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent each other.

6. (Original) The semiconductor device according to claim 2, wherein the dummy pattern has the same shape as a wiring for gate electrode.

7. (Currently Amended) A pattern layout method of a semiconductor device arranged with plural output bits comprising ~~the step of~~:

forming a dummy pattern having the same shape as the output bits to be adjacent to an end portion of an output bit group.

8. (Currently Amended) A pattern layout method of a semiconductor device arranged with plural output one bits and constituting an output bit group comprising ~~the step of~~:

forming a dummy pattern having the same shape as the output bits to be adjacent to an end portion of the output bit group.

9. (Original) The pattern layout method of a semiconductor according to claim 8, wherein the dummy pattern is formed at an empty space in a region where the plural output bits are arranged.

10. (Original) The pattern layout method of a semiconductor according to claim 8, wherein the dummy pattern is formed to be adjacent to the end portion of each output bit group constituting a cathode driver, an anode driver, and an anode driver for icon.

11. (Original) The pattern layout method of a semiconductor according to claim 10, wherein number of outputs of the dummy pattern formed at a region where output bit groups constituting the cathode driver, the anode driver, and the anode driver for icon are adjacent each other is less than number of outputs of the dummy pattern formed at a region where output bit groups are not adjacent each other.

12. (Original) The pattern layout method of a semiconductor according to claim 8, wherein the dummy pattern has the same shape as a wiring for gate electrode.